

**REMARKS**

**I. Introduction**

In response to the pending Office Action, Applicants respectfully traverse the pending rejection for the reasons set forth below.

**II. The Rejection Of The Claims Under 35 U.S.C. § 103**

Claims 1-11 were rejected under 35 U.S.C. § 103 as being obvious over USP No. 6,886,152 to Kong. Applicants respectfully submit that the pending claims are patentable over Kong for at least the following reasons.

Prior to discussing the prior art, a brief discussion of the present invention is provided. The present invention relates to a method for designing a semiconductor circuit which allows for the reduction in the power consumption of the resulting circuit. As discussed in the background portion of the specification, prior art design methods utilized devices having large design margins so that the designer could be assured that the design would work for the worst case conditions. However, such devices having high design margins have large power requirements during operation, thereby increasing the overall power requirements of the resulting circuit. The method of the present invention provides an efficient way of minimizing the necessary design margins of the devices so as to reduce overall power requirements of the resulting circuit, while simultaneously satisfying proper circuit operation.

More specifically, the method of the present inventions allows for the insertion of a load-dividing buffer at a position subsequent to a branching point and for the reduction of the drive capability of the drive cell disposed preceding the branching point. As a result of this process, excessive design margins provided for drive cells located prior to branching points, which were

provided in order to satisfy timing constraints of a given line of the multiple lines associated with the given branching point, can be reduced, as the newly inserted load-dividing buffer can drive the critical line, and the drive cell (now having reduced design margin) can drive the non-critical lines associated with the given branching point. A specific example of the method of the present invention is set forth in paragraphs [0048] to [0052] of the specification.

Turning to the claims, claim 1 recites in-part the steps of: (1) detecting a branch point of a wire in the layout; (2) virtually inserting a load at a predetermined point on one of the wires subsequent to the detected branching point; (3) calculating a delay amount of each route connecting cells via the branching point with the load being inserted and a delay amount without the load being inserted; (3) determining, based on the delay amount of each route, an insertion point at which a load-dividing buffer is to be inserted; (d) calculating a drive capability of a driving cell preceding the insertion point, and (e) deciding whether the load-dividing buffer is insertable at the insertion point.

Turning to the cited prior art reference, it is respectfully submitted that Kong wholly fails to disclose or suggest any of the foregoing limitations. First, Kong is related to a method for determining a satisfactory routing layout. There is no mention or suggestion in Kong of attempting to reduce the design margins of the drive cells utilized in the circuit design. One of the main objectives of the routing process of Kong is to route or re-route all of the non-critical loads through the driver with the largest “slack” (i.e., available drive capacity), *see*, col. 6, lines 50-59 of Kong. The “branching penalties” of Kong appear to be assigned values to wire segments, which can be arbitrarily assigned by the router, and which are utilized to determine which nodes critical and non-critical segments will be routed through, *see*, col. 6, lines 59-65 of Kong. Upon review, it is clear that Kong provides a method of determining the routing layout of

a circuit design. Kong does not disclose or suggest any method of reducing the power requirements of the drive cells contained within the design. In this regard, it is noted that the present invention could be utilized after the routing layout process has been completed, whereas Kong is specifically directed at a routing layout process.

At a minimum, Kong fails to disclose or suggest the following elements of claim 1. Kong fails to disclose the step of virtually inserting a load at a predetermined point on one of the wires subsequent to the detected branching point. Nowhere does Kong disclose or suggest inserting a virtual load into the circuit design. The pending rejection suggests that a rerouting algorithm of Kong corresponds to this claimed process step. It is not clear exactly how to respond to this suggestion. The two are wholly unrelated to one another. Kong discloses changing the routing of signals and determining if the resulting delays are within tolerance in an effort to determine an acceptable routing layout. The foregoing element of claim 1 recites virtually inserting a load on one of the wires located subsequent to the branch point. It cannot be properly concluded that Kong discloses this process step based on the disclosure of an unrelated algorithm.

Kong also fails to disclose the step of calculating a delay amount of each route connecting cells via the branching point with the load being inserted and a delay amount without the load being inserted. There is simply no disclosure in Kong that could be deemed as corresponding to this process step. Kong does not disclose inserting a virtual load, much less making two delay calculations in the same routing line, one with the virtual load present and the other with the virtual load removed.

Kong also fails to disclose the step of determining, based on the delay amount of each route, an insertion point at which a load-dividing buffer is to be inserted. Kong does not disclose

inserting a buffer into the circuit design. The portion of Kong cited in the Office Action is wholly silent with respect to inserting buffers with the layout design.

As each and every limitation must be disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (M.P.E.P. § 2143.03), and Kong clearly fails to do so, it is respectfully submitted that claim 1 is patentable over Kong. It is also submitted that claim 9 is patentable over Kong for at least the same reasons as discussed above.

In the event that the pending rejection is maintained, it is respectfully requested that the Examiner expressly identify where each of the process elements recited by claim 1 are disclosed in Kong so as to allow the Applicants an opportunity to fully and precisely respond to the rejection.

### **III. All Dependent Claims Are Allowable**

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

### **IV. Conclusion**

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If

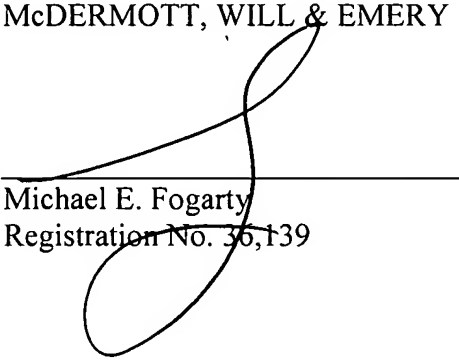
there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 9/20/05

By:   
Michael E. Fogarty  
Registration No. 36,139

600 13th Street, N.W. , Suite 1200  
Washington, D.C. 20005-3096  
Telephone: 202-756-8000 MEF/rp  
Facsimile: 202-756-8087

WDC99 1135879-1.069804.0015